

## **REMARKS**

### *1. No Motivation to Combine Tetrick with Fujihara et al.*

Claims 1 and 22 were rejected as allegedly being obvious over Tetrick in view of Fujihara et al. Applicants traverse this rejection, because there is no motivation or suggestion to combine the teachings of Tetrick with Fujihara et al. to provide the claimed invention. Tetrick explicitly teaches away from performing the functions of the claimed invention. Specifically, claim 1 defines a method as including, *inter alia*, a first controller monitoring operation of a processor to terminate the transmission of the data to the second random access memory location, during transmission of the quantity thereto, in response to the processor generating a write request to the second random memory location. Claim 22 defines a method that includes, *inter alia*, terminating the transmission of data to a second random access memory location, during transmission of a quantity thereto, in response to the processor generated a write request to the second random access memory location.

Tetrick, on the other hand, explicitly teaches away from these features by advocating deferring write cycles to a second memory address when copying data between first and second memory addresses. (See col. 6, lines 44-47). Modifying Tetrick to include the features of Fujihara et al. to provide the claimed invention would go against the explicit teachings of Tetrick. Therefore, it is respectfully submitted that a *prima face* case of obviousness is not present with respect to claims 1 and 22.

### *2. Claim 31*

Claim 31 has been amended to define a computer system including, *inter alia*, a volatile storage device having a plurality of locations for volatile storage of data, the controller being responsive to a command received from the processor to copy data from a first of the plurality of memory locations to a second of the plurality of memory location, and responsive to memory access requests from the processor to determine a delay in access by the processor to one of the first and second memory locations, with the delay being dependent upon a type of the request and the location among the first and second memory locations to which the access is directed, with the request being selected from a set of requests including a write request directed to the second memory location with the controller being responsive to the write request to terminate a transmission of a quantity of

data to the second random access memory location, during transmission of the quantity, in response to the write request. Applicants contend that Tetrick teaches away from a write request directed to the second memory location with the controller being responsive to the write request to terminate a transmission of a quantity of data to the second random access memory location, during transmission of the quantity, in response to the write request for the reasons stated above with respect to claims 1 and 22. As a result, Applicants contend that a *prima facie* case of obviousness is not present with respect to claim 31, as amended.

### 3. Dependent Claims

Considering that the dependent claims include all of the features of the independent claims from which they depend, the dependent claims are patentable to the extent that the independent claims are patentable. As a result, Applicants respectfully contend that a *prima facie* case of obviousness is not present with respect to the dependent claims for the reasons set forth above with respect to the independent claims from which they depend.

Therefore, Applicants respectfully request further examination in view of the amendments and remarks set forth above. A Notice of Allowance is earnestly solicited. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP438). If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6910.

Respectfully submitted,  
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